CLAIMS

What is claimed is:

1. Method for tuning a PLL circuit in which
   - a control voltage (VC), which is generated from a phase detector (PD) by means of a loop filter (SF), determines the output frequency (FO) of an oscillator (VCO), and
   - the output frequency (FO) in the phase detector (PD) is compared with a desired frequency (FR),

   wherein
   - the control voltage (VC) is increased in a first operating mode until the output frequency (FO) matches the desired frequency (FR) or, provided the control voltage (VC) reaches a first threshold value,
   - the control voltage (VC) is decreased in a second operating mode until the output frequency (FO) matches the desired frequency (FR) or, provided the control voltage (VC) reaches a second threshold value, is switched into the first operating mode.

2. Method according to claim 1, **wherein** the change in the control voltage (VC) in the first operating mode is performed by means of a current source (IQ) and in the second operating mode by means of a current sink (IS), and their currents overlay with the current from the phase detector (PD).

3. Method according to claim 2, **wherein** the control voltage (VC) is held constant when the output frequency (FO) matches the desired frequency (FR), while the current of the phase detector (PD) compensates the current of the current source (IQ) or the current of the current sink (IS).

4. Method according to claim 3, **wherein** the control voltage (VC) is modulated provided the output frequency (FO) does not match the desired frequency (FR), while the phase detector (PD) supplies a temporally variable current to the loop filter (SF) the frequency of which is proportional to the size of the difference between the output frequency (FO) and the desired frequency (FR).

5. Method according to claim 4, **wherein** the maximum amplitude of the current of the phase detector (PD) is greater than the amplitude of the current from the current source (IQ)) or the current sink (IS).

6. Method according to claim 5, **wherein** the maximum amplitude of the current of the phase detector (PD) falls as the difference between the desired frequency (FR) and output frequency (FO) increases.

7. Method according to claim 6, **wherein** the modulation amplitude of the control voltage (VC) is damped by a low pass characteristic of the loop filter (SF).

8. Cancelled

9. Cancelled

10. Cancelled

11. (new) Method according to claim 1, wherein the phase detector (PD) generates a control signal (LD) to indicate that the output frequency (OF) matches the desired frequency (FR).

12. (new) PLL circuit arrangement for implementing the method according to claim 1, comprising

a phase detector (PD) which is linked to a loop filter (SF),

a voltage-controlled oscillator (VCO) which is wired to the loop filter (SF),

at least one control unit (ST) which is linked to the loop filter (SF) and the phase detector (PD) in order to monitor the control voltage (VC) of the oscillator (VCO), and

a current source (IQ) and a current sink (IS) which are linked to the loop filter (SF) by means of a switching element (E).

13. (new) PLL circuit arrangement according to claim 12, wherein the control unit (ST) for comparing the control voltage with the two threshold values has at least one comparator and has at least one memory unit for storing the operating state.